



A large, detailed image of a microchip die is positioned diagonally across the top half of the slide. The die is a complex grid of various colored squares (red, orange, yellow, green, blue, and purple) representing different functional blocks and interconnects. A small, bright green chevron points towards the bottom right corner of the die.

MOTIVATION AND STRATEGY FOR A NEW ABSTRACT MEMORY INTERFACE

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STANDARDS & INNOVATION

Memory systems are where the interesting key innovation will occur in the coming years

- ▲ A good standard enables innovation and significantly benefits the industry
- ▲ An overly restrictive standard stifles innovation
- ▲ An irrelevant standard is a waste of effort
 - Read Wikipedia article on the failure of Futurebus for a sobering example.

Goal:

Develop a high volume commercial standard that enables ongoing innovation and also meets the needs of exascale systems.

MOTIVATION BASED ON COMPANY TYPE

Memory Companies:

- ▲ Are *ALL* highly motivated to move up the value chain and produce something with value added IP.

Processor Companies:

- ▲ Want all value added IP to be on the processor chip, with memory remaining low-cost vanilla commodity parts
 - Have good experience and IP for optimizing memory controllers
- ▲ But cannot afford to design a new memory interface for every new memory technology and architecture coming down the pipeline

System Companies:

- ▲ Would like the flexibility to assemble unique value added systems

THE JEDEC STANDARDS PROCESS

- ▲ The ultimate endorsement for a high volume memory standard
- ▲ JEDEC is optimized for controlled incremental improvements
 - DDR4: 8 years from first presentation to first commercially available parts
- ▲ May never agree on a DDR5 standard
- ▲ But can it agree on a revolutionary new standard in any reasonable time?
 - Standards process first, or working parts first?
- ▲ How do we get key companies to view such a new standard as being in their *best business interest* ??

RELATION TO OTHER PROTOCOLS

Can we think of this as a follow-on extension to:

- ▲ IBM's CAPI effort
- ▲ AMD's Coherent Hyper-Transport
- ▲ Intel's QPI
- ▲ RapidIO

They are all trying to do some aspects of the same thing

What are the lessons to be learned from failed attempts:

- ▲ Futurebus
- ▲ Scalable Coherent Interface (SCI)

RELATION TO FAST FORWARD - 2

▲ AMD Press release on FF2 (in part):

“...AMD will collaborate with the DOE *and others* to help define a new standard for memory interfaces that meets the needs of future-generation memory devices, including non-volatile memory and processing-in-memory (PIM) architectures...”

▲ Press releases from other companies are still pending

WHERE DO WE GO FROM HERE?

1. Define organizational goals, scope, membership, and plan for a study / advocates group
2. Learn lessons from past attempts at this
3. Define the technical goals, scope and high level outline of a new standard
4. ★ Work on developing buy-in from some key industry players ★
5. Get criticized in editorials in key industry magazines
6. Disrupt the entire computer ecosystem